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10/620,470	07/15/2003	Lawrence T. Clark	42P17468	8637

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,470	CLARK, LAWRENCE T.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received July 15, 2003 for application number 10/620,470. The Office hereby acknowledges receipt of the following and placed of record in file: Specification, Drawings, Abstract, Oath/Declaration and Claims 1-22 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kolinski et al. (U.S. Patent No. 6,092,207) (hereinafter referred to as Kolinski).

As to claim 1, Kolinski discloses a method, comprising: moving integrated circuit state into on-die storage (DRAM 265) and externally disabling power (via 210) to on-die combinational circuitry (285) (column 4, lines 23-43 and column 4, lines 55-67 and column 5, lines 46-57).

As to claim 3, Kolinski further discloses the method of claim 1, wherein disabling power further includes gating an off-die clamp to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry (via switches 230, 232, 250 and 252) (column 2, line 57 thru column 3, line 15 and column 3, line 63 thru column 4, line 22).

As to claim 5, Kolinski further discloses the method of claim 1, further including reapplying power after the integrated circuit receives an interrupt (column 6, lines 18-29).

As to claim 6, Kolinski further discloses the method of claim 1, further including: supplying the power from a power supply regulator along a path to the on-die combinational circuitry; and providing a feedback signal (332) from the path to the power supply regulator (column 3, line 63 thru column 4, line 10 and column 4, lines 55-67 and column 5, lines 26-45).

Claims 7, 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Stapleton et al. (U.S. Patent No. 6,574,577 B2) (hereinafter referred to as Stapleton).

As to claim 7, Stapleton discloses a method comprising: forcing a high impedance state on an output of a power supply regulator (11) that is coupled to a power pin of an integrated circuit (12) (column 1, lines 40-57 and column 2, lines 38-50).

As to claim 8, Stapleton further discloses the method of claim 7 wherein forcing a high impedance state further includes: de-asserting a drive pin coupled to a gate of a MOS power transistor to force the high impedance state on the output of the power supply regulator (column 2, lines 38-50).

As to claim 10, Stapleton further discloses the method of claim 7 further comprising: timing the de-assertion to avoid high voltages on a supply inductor coupled between the output of the power supply regulator and the power pin of the integrated circuit (Abstract and column 2, lines 1-10).

Claims 11 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson et al. (U.S. Patent No. 5,999,386) (hereinafter referred to as Anderson).

As to claim 11 Anderson discloses a circuit comprising: a first terminal (124) of an integrated circuit coupled to receive power when the integrated circuit is in an active mode and not receive power when the integrated circuit is in a low power mode (column 6, lines 41-65); and a second terminal (30) to receive power supplied to circuitry (48) for low power state retention when the integrated circuit is in the low power mode (column 6, lines 41-65).

As to claim 17, Lu further discloses the circuit of claim 11 further comprising: a transistor internal to the integrated circuit to gate the power received at the first terminal and float an internal power conductor connected to combinational logic (column 8, lines 1-13).

Claims 18-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Lu et al. (U.S. Patent No. 6,064,223) (hereinafter referred to as Lu).

As to claim 18, Lu discloses a system comprising: an integrated circuit (106) having a power terminal coupled through an external control transistor to an output of a power supply (column 2, line 40 thru column 3, line 67 and column 5, lines 47-55).

As to claim 19, Lu further discloses the system of claim 18 wherein the control transistor is an NMOS transistor (column 2, line 40 thru column 3, line 67).

As to claim 20, Lu further discloses the system of claim 18 wherein the control transistor is a CMOS pass gate (column 2, line 40 thru column 3, line 67).

As to claim 21, Lu further discloses the system of claim 18 further including: a multiplexer to couple a power signal supplied at a pin of the integrated circuit to the power supply while the integrated circuit operates in an active mode (column 2, line 63 thru column 3, line 4).

As to claim 22, Lu further discloses the system of claim 21 wherein the multiplexer disconnects the power signal from the power supply while the integrated circuit is in a low power standby mode (column 3, line 65 thru column 4, line 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kolinski (as cited above) as applied to claim 1 above, and further in view of Stapleton (as cited above).

As to claim 2, Kolinski fails to disclose the method wherein disabling power further includes tri-stating an output of a power supply regulator.

Stapleton teaches a power regulator circuit (11) that tri-states its output to an integrated circuit (processor 12) (column 1, lines 41-57 and column 2, lines 38-50). Stapleton has the

additional benefit of using a voltage identification number (VID) to identify the any needed voltage level for the circuit based on the VID (column 1, lines 15-26).

It would have been obvious to one of ordinary skill of the art having the teachings of Kolinski and Stapleton at the time the invention was made, to modify the power supply of Kolinski to include the ability to tri-state the voltage output as taught by Stapleton. One of ordinary skill in the art would be motivated to make this combination of tri-stating the output voltage of the voltage regulator in view of the teachings of Stapleton, as doing so would give the added benefit of using a voltage identification number (VID) to identify the any needed voltage level for the circuit based on the VID (as taught by Stapleton above).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kolinski (as cited above) as applied to claim 1 above, and further in view of Anderson (as cited above).

As to claim 4, Kolinski fails to disclose the method wherein disabling power further includes gating an on-die clamp to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry.

Anderson teaches an IC that has the capability using an on-die clamp (130) to disrupt power supplied from an external power supply regulator (via 124) to the on-die combinational circuitry (column 6, lines 24-65). Anderson has the additional feature of having on-chip electrostatic discharge protection circuitry (column 5, lines 25-40).

It would have been obvious to one of ordinary skill of the art having the teachings of Kolinski and Anderson at the time the invention was made, to modify the power lines of Kolinski to include on-die clamps to disrupt power as taught by Anderson. One of ordinary skill in the art would be motivated to make this combination of including on-die clamps to disrupt

power in view of the teachings of Anderson, as doing so would give the added benefit of having on-chip electrostatic discharge protection circuitry (as taught by Anderson above).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stapleton (as cited above) as applied to claim 7 above, and further in view of Cruz (U.S. Patent No. 6,754,692 B2) (hereinafter referred to as Cruz).

As to claim 9, Stapleton fails to further disclose the method further comprising: connecting a diode to a source of the MOS power transistor.

Cruz teaches a power distribution circuit (100) that includes a diode (140) which keeps current from flowing into a circuit's power supply system which is inclusive of a MOS transistor (170) (column 2, lines 24-60 and column 6, lines 14-29). Cruz further teaches the additional benefit of electronically isolating power buses from power domains (column 1, lines 33-53 and column 2, lines 49-60).

It would have been obvious to one of ordinary skill of the art having the teachings of Stapleton and Cruz at the time the invention was made, to modify power supply regulator of Stapleton to include a diode to a source MOS power transistor as taught by Cruz. One of ordinary skill in the art would be motivated to make this combination of including a diode in the power supply regulator in view of the teachings of Cruz, as doing so would give the added benefit of electronically isolating power buses from power domains (as taught by Cruz above).

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (as cited above) as applied to claim 11 above, and further in view of Massie (U.S. Patent No. 5,678,049) (hereinafter referred to as Massie).

As to claim 14, Anderson fails to disclose the circuit wherein a feedback signal is taken from the first terminal and supplied to a power regulator.

Massie teaches a method and apparatus that remotely controls and monitors the power supply (125) of a circuit (105) wherein a feedback loop is used to detect power delivered to the circuit at the pin of the circuit (column 3, lines 6-12 and column 6, lines 1-17). Massie has the additional benefit of supplying power to an IC having uncommon operating voltages without the need for system power supply redesign (column 1, lines 32-43).

It would have been obvious to one of ordinary skill of the art having the teachings of Anderson and Massie at the time the invention was made, to modify the circuit of Anderson to include a feedback signal to the power regulator from the terminal of the IC as taught by Massie. One of ordinary skill in the art would be motivated to make this combination of including a feedback signal to the power regulator from the terminal of the IC in view of the teachings of Massie, as doing so would give the added benefit of supplying power to an IC having uncommon operating voltages without the need for system power supply redesign (as taught by Massie above).

As to claim 15, Anderson fails to disclose the circuit wherein a feedback signal is taken from within the integrated circuit and supplied to a power regulator.

Massie teaches a method and apparatus that remotely controls and monitors the power supply (125) of a circuit (105) wherein a feedback loop is used to detect power delivered to the circuit from within the circuit (column 3, lines 6-12 and column 6, lines 1-17). Massie has the additional benefit of supplying power to an IC having uncommon operating voltages without the need for system power supply redesign (column 1, lines 32-43).

It would have been obvious to one of ordinary skill of the art having the teachings of Anderson and Massie at the time the invention was made, to modify the circuit of Anderson to include a feedback signal to the power regulator from within the IC as taught by Massie. One of ordinary skill in the art would be motivated to make this combination of including a feedback signal to the power regulator from within the IC in view of the teachings of Massie, as doing so would give the added benefit of supplying power to an IC having uncommon operating voltages without the need for system power supply redesign (as taught by Massie above).

Claims 12, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson as applied to claim 11 above, and further in view of Lu (as cited above).

As to claim 12, Anderson does not disclose the circuit further comprising: a transistor external to the integrated circuit to gate the power received at the first terminal.

Lu teaches a MOSFET circuit (Fig. 2) external to a logic device (106) that is capable of gating off power to an unused circuit (column 2, lines 3-10 and column 5, lines 47-55). Lu further teaches the circuit comprising a transistor (102) external to the integrated circuit to gate the power received at the first terminal (column 2, lines 40-67 and column 3, line 65 thru column 4, line 8). Lu teaches the additional benefit of reducing leakage current when the circuit is gated off (column 1, lines 35-36 and column 2, lines 3-10).

It would have been obvious to one of ordinary skill of the art having the teachings of Anderson and Lu at the time the invention was made, to modify circuit of Anderson to include an external transistor to gate the power received by the IC as taught by Lu. One of ordinary skill in the art would be motivated to make this combination of including an external transistor to gate

the power received by the IC in view of the teachings of Lu, as doing so would give the added benefit of reducing leakage current when the circuit is gated off (as taught by Lu above).

As to claim 13, Anderson in combination with Lu taught the circuit in claim 12, as shown above. Lu further teaches the circuit wherein the transistor is coupled to a power regulator and switched off when the integrated circuit is in the low power mode (column 2,lines 40-67).

As to claim 16, Anderson does not disclose the circuit further including a multiplexer to receive a signal taken from within the integrated circuit and a signal external to the integrated circuit, where an output of the multiplexer is coupled to a power regulator.

Lu teaches a MOSFET circuit (Fig. 2) external to a logic device (106) that is capable of gating off power to an unused circuit (column 2, lines 3-10 and column 5, lines 47-55). Lu further teaches the circuit further including a multiplexer to receive a signal taken from within the integrated circuit and a signal external to the integrated circuit, where an output of the multiplexer is coupled to a power regulator (column 2, line 40 thru column 3, line 4). Lu teaches the additional benefit of reducing leakage current when the circuit is gated off (column 1, lines 35-36 and column 2, lines 3-10).

It would have been obvious to one of ordinary skill of the art having the teachings of Anderson and Lu at the time the invention was made, to modify circuit of Anderson to include an external transistor to gate the power received by the IC as taught by Lu. One of ordinary skill in the art would be motivated to make this combination of including an external transistor to gate the power received by the IC in view of the teachings of Lu, as doing so would give the added benefit of reducing leakage current when the circuit is gated off (as taught by Lu above).

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
October 28, 2006